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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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COOK, ALEX, MCFARRON, MANZO,
CUMMINGS & MEHLER, LTD.
Suite 2850
200 West Adams St.
Chicago, IL 60606

EXAMINER
PHAM, THANH V

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 05/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/768,133	NAGAO ET AL.	
	Examiner	Art Unit	
	Thanh V. Pham	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 April 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *See Continuation Sheet* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10, 12, 14, 16, 18, 20, 22, 24, 26, 28, 31, 33, 35-41, 43-50, 52-59, 61-68, 70-77, 79-86, 88-91, 93-95, 97-101, 103-105, 107-111, 113-115, 117-121, 123-125, 127, 129-131, 133-135, 137, 139-141, 143-145, 147, 149-152, 154-156, 158, 161-164, 166-168, 170, 173-176, 178-180, 182, 185-196* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *04/21/06,01/30/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Continuation of Disposition of Claims: Claims pending in the application are 1-10,12,14,16,18,20,22,24,26,28,31,33,35-41,43-50,52-59,61-68,70-77,79-86,88-91,93-95,97-101,103-105,107-111,113-115,117-121,123-125,127,129-131,133-135,137,139-141,143-145,147,149-152,154-156,158,161-164,166-168,170,173-176,178-180,182 and 185-196.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 04/21/2006 and 03/21/2006 have been entered.

Response to Amendment

Claim Rejections - 35 USC § 103

2. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

3. Claims 1-10, 12, 14, 16, 18, 20, 22, 24, 26, 28, 31, 33, 35-41, 43-50, 52-59, 61-68, 70-77, 79-86, 88-91, 93-95, 97-101, 103-105, 107-111, 113-115, 117-121, 123-125, 127, 129-131, 133-135, 137, 139-141, 143-145, 147, 149-152, 154-156, 158, 161-164, 166-168, 170, 173-176, 178-180, 182, 185-196 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art in combination with Chen U.S. Patent No. 5,453,406, Tang et al. US 5,550,066 and Hanihara et al. US 5,990,988.

The applicant's admitted prior art for the TFT formation to form a display device having pixel electrodes and an insulative layer over the pixel electrodes is similar to the

instant invention, having use of an organic material where a low dielectric property is considered (the instant specification, pages 1-2 and 7).

> An active matrix liquid crystal display device is widely used for OA equipment, television sets and the like.
>
> The substrate is spun so that the varnish is uniformly applied thereto. The substrate on which the varnish is applied is baked in an oven or on a hot plate to obtain an insulating film.
>
> The thickness of the insulating film is controlled by the number of spinnings, the period of spinning time, the concentration and the viscosity of the varnish. A material used for spin-coating can be selected from a polyimide resin, an acrylic resin, a resin containing a siloxane structure, an inorganic SOG (Spin on Glass) material and the like, in consideration of physical properties such as a transparence, a heat resistance, a chemical resistance, and a thermal expansion coefficient. In the case where a low dielectric property is considered as an important factor, an organic material is often used.
>
> FIG. 2 shows a cross section of a conventional active matrix substrate. On a glass substrate 100, level differences generated by an active layer (including a channel region 101, a source region 102, and a drain region 103), a gate wiring 105, a source wiring 107, a drain wiring 108 and the like are present. A leveling resin, representatively an acrylic resin, is used to as a first leveling film 109 so as to level these level differences. Finally, a pixel electrode 111 is formed on the first leveling film 109 to complete the active matrix substrate.
>
> Next, as shown in FIG. 3, the active matrix substrate is bonded to a counter substrate 120 so as to interpose liquid crystal 123 therebetween to form a liquid crystal display device. According to this conventional method of forming a leveling film, however, it is apprehended that the pixel electrode 111 might be broken because of insufficient flatness of the leveling film. Moreover, since the unevenness due to the level differences remains on the surface of the pixel electrode 111, poor orientation of the liquid crystal 123 is caused on the uneven region of the surface.

As being seen in fig. 2, the wiring is connected to the semiconductor film through a first hole in the interlayer insulating film on the interlayer insulating film and the pixel

electrode is connected to the wiring through a second hole. In applicant's admitted prior art fig.3, an electro luminescence layer 112 is formed over the pixel electrode 111.

In the Summary of the Invention, the instant specification states, "a TFT is formed in a similar manner as in the prior art shown in Fig. 2". However, the applicant's admitted prior art lacks the second leveling layer over the first leveling layer.

The Chen reference discloses a method for producing a planar surface (col. 2, lines 64-67) wherein the thickness of a first leveling film 40 (2,000-3,000 Angstroms, col. 6, lines 1-10) formed above a wiring 34 is thinner than that of a second leveling film 42 (4,000-6,000 Angstroms, col. 6, line 53-54) formed on the first leveling film. Both first and second leveling films are formed by spin coating and by the same material (col. 6, line 30). The method could be used to coat a display device.

In Chen's fig. 7, a second spin-on-glass layer 42 is formed over the first spin-on-glass layer 40 essentially planarizing the dielectric layer and completing the process. This second spin-on-glass layer 42 is formed by also using the liquid precursor of the siloxane type similar in composition to the material used for the first spin-on-glass layer 40, but in this second coating the spin-on-glass is dispensed at a significantly higher spin speed and at a constant speed. The same series of spin-on-glass is used for both layers. There are three consecutive sections related to the insulating layer and the first and second spin-on-glass layers. The first section in col. 5, lines 50-60 teaches the formation of the insulating layer 36 with "the preferred thickness of the insulating layer 36 is between about 2000 to 4000 Angstroms".

The second section, from col. 5, line 61 to col. 6, line 24, teaches the formation of the first spin-on-glass layer 40 with "more specifically the preferred spin-on-glass material is a series of siloxane base material" with an example of using series 211 which "produce a thinner coating of about 2000 Angstroms while series 314 and 311 have a higher viscosity and produce coatings of about 3000 Angstroms" in the conditions of

> First bringing the substrate to a constant rotational speed in the range of about 600 to 800 revolutions per minute (rpm) and then dispensing the spin-on-glass liquid precursor for about 6 seconds. The spin-on-glass is then allowed to air dry at room temperature of about 25 ^{O}C for another 15 second at the above constant rotational speed. The substrate is then removed from the spin coater and baked, for example on a hot plat, at a temperature of between about 100 to 300 for a time of between 0.5 to 2.0 minutes, because of this lower and constant spin speed the recesses or gaps between the patterned conductor 34 fill more evenly, as was depicted earlier in FIGS. 3A and 3B.

The third section in col. 6, lines 25-55 teaches the formation of the second spin-on-glass 42 in the conditions of "this second spin-on-glass layer 42 is formed by also using the liquid precursor of the siloxane type similar in composition to the material used for the first spin-on-glass layer 40, but in this second coating the spin-on-glass is dispensed at a significantly higher spin speed and at a constant speed" wherein

> The substrate is again placed on a spin coater and brought to a constant rotational speed in the range of about 2500 to 3000 revolutions per minute (rpm) before dispensing the spin-on-glass and then the substrate is maintained at this constant rotational speed for an additional 6 seconds. The substrate is then brought to a stationary position, that is the spin speed is reduced to zero rpm and the second spin-on-glass is allowed to air dry at room temperature of about 25 ^{O}C for an additional 15 seconds. The substrate is them baked, for example on a hot plate, at a temperature of between about 100 to 300 ^{O}C for a time of between about 0.5 to 2.0 minutes, the spin-on-glass layer 42 is then pyrolzed at a relatively high temperature to form an inorganic glass. The preferred curing temperature for this last step is between about 400 to 500 ^{O}C and for a time of about 20 to 30 minutes, and more specifically at a temperature of 425 ^{O}C for 30

> minutes thereby forming the inorganic glass. The preferred thickness of layer 42 is between about 4000 to 6000 Angstroms as can be seen in FIG. 7, the spin-on-glass dielectric layer fills the recesses and essentially planarizes the irregular recesses or gaps on the substrate.

It is clear that with the same composition put in different conditions, the thickness of the two spin-on-glass layers have different thickness. The example in the above second section in the formation of the first spin-on-glass/leveling layer 40 is about 2000 or 3000 Angstroms. The given thickness of the preferred series 211, 314 or 311 while teaching the first spin-on-glass formation is obviously the preferred thickness for that layer. The preferred thickness of layer 42 is not 2000 or 3000 Angstroms but preferred up to 4000 to 6000 Angstroms is formed thicker than the previous spin-on-glass layer.

Further, in its claims, the Chen reference discloses various thicknesses for the first and second 'leveling' layers separately. One of ordinary skill in the art could chose from the provided ranges to have the second leveling film thicker than the first leveling film as a matter of routine experimentation based on those provided ranges. Choice of thickness of the leveling layers would further depend on many other factors such as the gap between the protruded elements or the height of the protruded element and would be obtained by routine experimentation, MPEP 2144.05. It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the appropriate thickness such as the thickness in the ranges as claimed into the process as the thickness would be selected in accordance with the surface planarity formation as taught by Chen.

> *The Chen reference further discloses, col. 5, lines 24-29*

> insulating layer 32 is deposited thereon (on devices' conducting layers) by conventional means. For example, the insulating layer can be composed of silicon dioxide and silicon nitride and deposited using CVD or LPCVD.

and *col. 6, line 67 to col. 7, line 15*

> Although this embodiment describes a process for forming a single planar dielectric layer over a single patterned conducting layer, it should also be well understood by one skilled in the art that the process can be repeated to form additional patterned metal layers having planarized dielectric layer formed thereon. This can be accomplished by first depositing a second insulating barrier layer over the cured second spin-on-glass layer 42, forming via hole openings in the planar dielectric layer to the underlying conducting layer and then depositing a second conducting layer, such as aluminum, which contacts the first conducting layer through the via holes, the conducting layer can then be patterned by reactive ion etching and then planarizing process ARIC SOG of this invention can be used to planarize the second level metal. By repeating this process by the above method a multilayered metallurgy can be fabricated.

The passivating layer of an insulating material such as silicon oxide (Tang et al., col. 7, line 30), silicon nitride or silicon oxide (Chen, col. 5, lines 24-27) as same as "Specific insulators include noncrystalline compounds such as silicon oxide, silicon nitride, or silicon nitride oxide," Nishimura et al. US 6,332,835, col. 7, lines 64-6 and/or "the insulating film formed on the data line, not only an oxide film, but also a nitride film or oxide-nitride film may be used", Tsuji et al. US 5,821,622, col. 27, lines 2-4, is well known in the art.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the applicant's admitted prior art with the second leveling layer as taught by Chen because the second leveling layer of Chen would provide the prior art structure with planarity over the formed TFT to prevent the pixel electrode from rough topography and improve the optical resolution (Chen's col. 1, lines 18 and 29). With this combination, the pixel electrode would be connected to the wiring through a

second hole formed in the passivating/insulating film (of silicon nitride, silicon oxide nitride or silicon oxide as well-known in the art) and the leveling film on the wiring as claimed.

Re claim 8, the applicant's admitted prior art discloses the driving TFT section but not the section of pixel TFT for controlling electric current to the EL element therefore it does not show the EL cathode. However, the formation of a cathode made of a conductive film having a light shielding property is known in the art as EL cathode 84 in the Tang et al.'s figs. 3 and 9 and the associated passages. The Tang et al. reference also teaches "a passivating layer 74 of an insulating material, preferably silicon dioxide, is deposited over the surface of the device (the wiring 62/72)" (col. 7, lines 30-35).

It would have been obvious to one of ordinary skill in the art at the time of the invention to provide the method of the combination with the formation of a cathode made of a conductive film having a light shielding property of Tang et al. because the formation of a cathode made of a conductive film having a light shielding property of Tang et al. would provide the method of the combination with sufficiently low temperature fabrication (abstract and col. 2, line 61, e.g.)

The applicant's admitted prior art does not disclose the wiring is a three-layered laminated film containing a first titanium, an aluminum film and a second titanium film. The Hanihara et al. reference teaches "the wiring layers 31, 32,33 and the pixel electrode layer 34 are films made of such conductive metals as ... layers of titanium and aluminum formed by sputtering or evaporation or photolithography" (col. 6, lines 18-24). It would have been obvious to one of ordinary skill in the art at the time of the invention

to provide the method of the combination with the layers of titanium and aluminum as taught by Hanihara et al. because the layers of titanium and aluminum for the wiring would provide the device formed by the combination with controllability (col. 1, line 9).

Response to Arguments

4. Applicant's arguments filed 04/24/2006 and 03/21/2006 have been fully considered but they are not persuasive. The main issue in the argument is about the thicknesses of the two leveling films (03/21/2006 remark's pages 35-36).

Applicant is directed to the passages from col. 5, line 50 to col. 6, line 55 in the Chen reference which can be divided into three sections as pointed out in the rejection section. The Chen reference considered as a whole in the above rejection is the response to the argument.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh V. Pham whose telephone number is 571-272-1866. The examiner can normally be reached on M-Th (6:30-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TWP
05/03/2006

George Fourson
Primary Examiner